IS31AP4066D

DUAL 1.3W STEREO AUDIO AMPLIFIER

December 2011

GENERAL DESCRIPTION

The IS31AP4066D is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 1.3W to an 8Ω load.

The IS31AP4066D features a low-power consumption shutdown mode and thermal shutdown protection. It also utilizes circuitry to reduce "click-and-pop" during device turn-on.

APPLICATIONS

- Cell phones, PDA, MP4,PMP
- Portable and desktop computers
- Desktops audio system
- Multimedia monitors

KEY SPECIFICATIONS

- P_O at R_L = 8Ω, V_{DD} = 5V
  THD+N = 1% ---------------------- 1.3W (Typ.)
  THD+N = 10% --------------------- 1.6W (Typ.)
- P_O at R_L = 8Ω, V_{DD} = 4V
  THD+N = 1% ----------------------- 0.81W (Typ.)
- Shutdown current ------------------- 0.3µA (Typ.)
- Supply voltage range --------------- 2.7V ~ 5.5V
- QFN-16 (3mm × 3mm) package

FEATURES

- Suppress "click-and-pop"
- Thermal shutdown protection circuitry
- Micro power shutdown mode

TYPICAL APPLICATION CIRCUIT

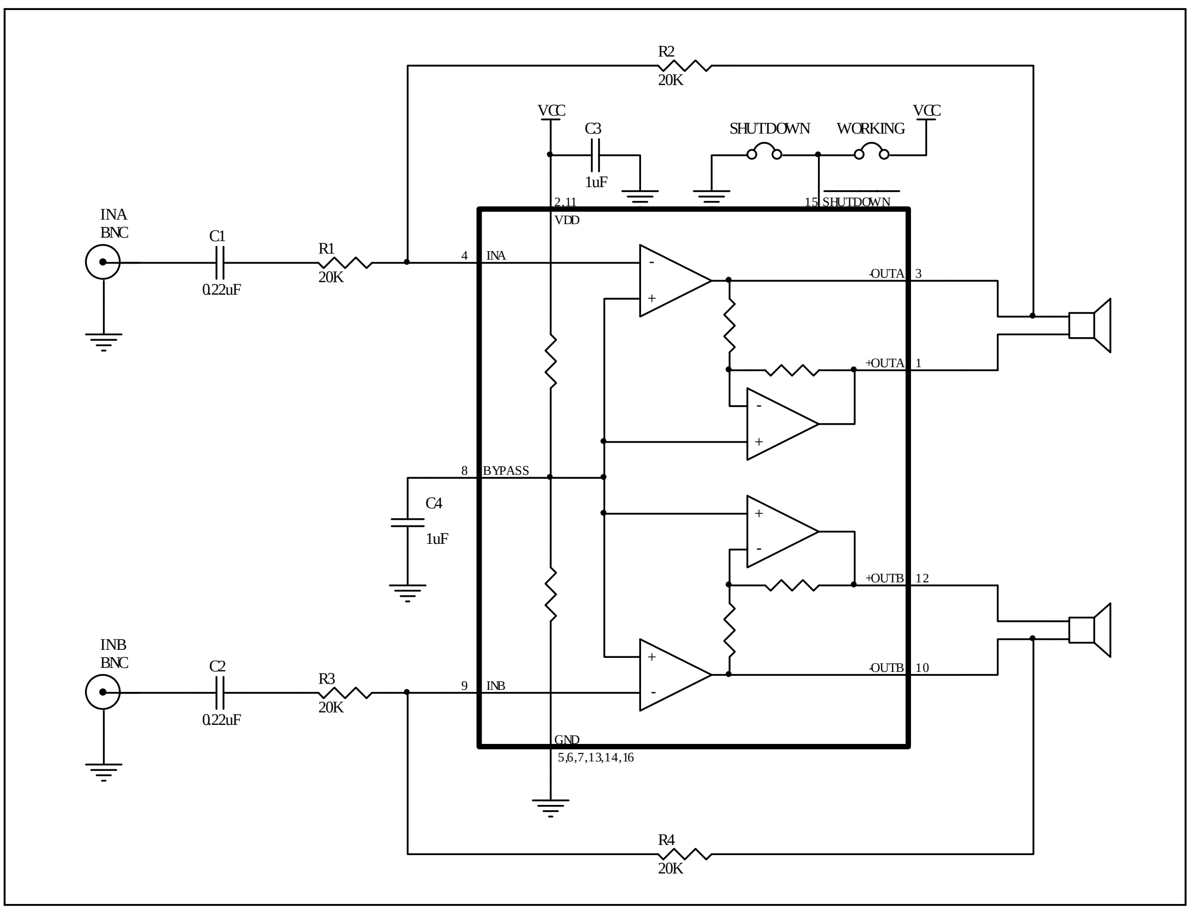
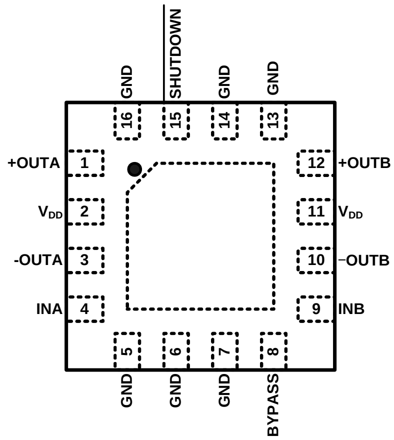


Figure 1 Typical Application Circuit

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-16	

PIN DESCRIPTION

No.	Pin	Description
1	+OUTA	Left channel +output.
2,11	V_{DD}	Supply voltage.
3	-OUTA	Left channel –output.
4	INA	Left channel Input.
5~7,13,14,16	GND	GND.
8	BYPASS	Bypass capacitor which provides the common mode voltage.
9	INB	Right channel input.
10	-OUTB	Right channel –output.
12	+OUTB	Right channel +output.
15	$\overline{\text{SHUTDOWN}}$	Shutdown control, hold low for shutdown mode.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31AP4066D-QFLS2-TR	QFN-16, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	−0.3V ~ +6.0V
Voltage at any input pin	−0.3V ~ V_{DD}+0.3V
Junction temperature, T_{JMAX}	−40°C ~ +150°C
Storage temperature range, Tstg	−65°C ~ +150°C
Operating temperature ratings	−40°C ~ +85°C
Solder information, Vapor Phase (60s) Infrared (15s)	215°C 220°C

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{DD}= 5V, unless otherwise noted.
Limits apply for T_A = 25°C. (Note 1 or specified)

Symbol	Parameter	Condition	Typ.	Limit	Unit
V_{DD}	Supply voltage			2.7	V(min)
				5.5	V(max)
I_{DD}	Quiescent power supply current	V_{IN} = 0V, Io = 0A	3.9	10.0	mA(max)
I_{SD}	Shutdown current	GND applied to the shutdown pin	0.3	2.5	μA(max)
V_{IH}	Shutdown input voltage high			1.4	V(min)
V_{IL}	Shutdown input voltage low			0.4	V(max)
T_{WU}	Turn on time	1μF bypass cap(C4) (Note 2)	120.0		ms

ELECTRICAL CHARACTERISTICS OPERATION

The following specifications apply for V_{DD}= 5V, unless otherwise noted.
Limits apply for T_A = 25°C. (Note 2 or specified)

Symbol	Parameter	Condition	Typ.	Limit	Unit
Vos	Output offset voltage	V_{IN} = 0V	5.0	25.0	mV(max)
Po	Output power	THD+N = 1%, f = 1kHz, R_L= 8Ω	1.3		W(min)
		THD+N = 10%, f = 1kHz, R_L = 8Ω	1.6		W(min)
THD+N	Total harmonic distortion +noise	1kHz, Avd = 2, R = 8Ω, Po = 1W	0.1		%
PSRR	Power supply rejection ratio	Input floating, 217Hz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	80.0		dB
		Input floating 1kHz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	70.0		dB
		Input GND 217Hz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L =8Ω	60.0		dB
		Input GND 1kHz V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	60.0		dB
X_{talk}	Channel separation	f = 1kHz, C4 = 1μF	-100.0		dB
V_{NO}	Output noise voltage	1kHz, A-weighted	7.0		μV

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{DD}= 3V, unless otherwise noted.
Limits apply for T_A = 25°C. (Note 1 or specified)

Symbol	Parameter	Condition	Typ.	Limit	Unit
I_{DD}	Quiescent power supply current	V_{IN} = 0V, I_O = 0A	2.6	6.5	mA(max)
I_{SD}	Shutdown current	GND applied to the shutdown pin	0.1	2.2	μA(max)
V_{IH}	Shutdown input voltage high			1.1	V(min)
V_{IL}	Shutdown input voltage low			0.4	V(max)
T_{WU}	Turn on time	1μF bypass cap(C4) (Note 2)	110		ms

ELECTRICAL CHARACTERISTICS OPERATION

The following specifications apply for V_{DD}= 3V, unless otherwise noted.
Limits apply for T_A = 25°C. (Note 2 or specified)

Symbol	Parameter	Condition	Typ.	Limit	Unit
Vos	Output offset voltage	V_{IN}=0V	2.5	25.0	mV
Po	Output power	THD+N = 1%, f = 1kHz, R_L= 8Ω	0.5		W
		THD+N = 10%, f = 1kHz, R_L = 8Ω	0.6		W
THD+N	Total harmonic distortion+noise	1kHz, Avd = 2, R_L = 8Ω, Po = 0.3W	0.1		%
PSRR	Power supply rejection ratio	Input floating, 217Hz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	75.0		dB
		Input floating 1kHz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	70.0		dB
		Input GND 217Hz, V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L =8Ω	62.0		dB
		Input GND 1kHz V_{ripple} = 200mV_{p-p} C4 = 1μF, R_L = 8Ω	62.0		dB
X_{talk}	Channel separation	f = 1kHz, C4 = 1μF	-100.0		dB
V_{NO}	Output noise voltage	1kHz, A-weighted	7.0		uV

Note1: All parameters are production tested at 25°C, functional operation of the device and parameters specified over other temperature range, are guaranteed by design, characterization and process control.

Note 2: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

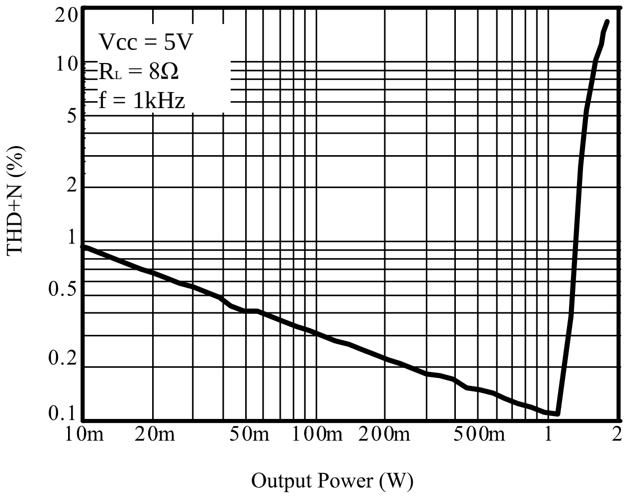


Figure 2 THD+N vs. Output Power

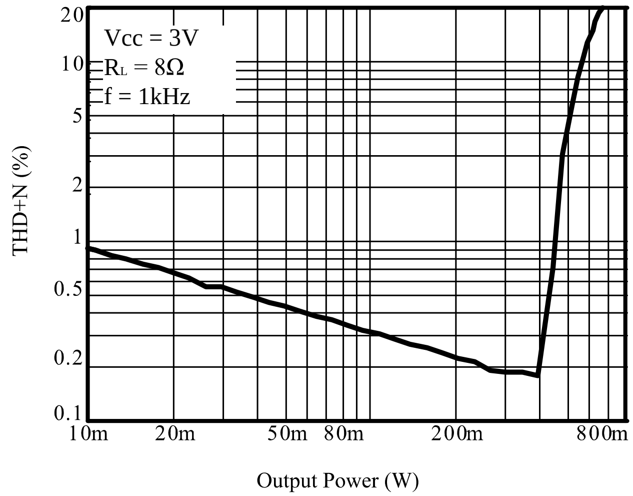


Figure 3 THD+N vs. Output Power

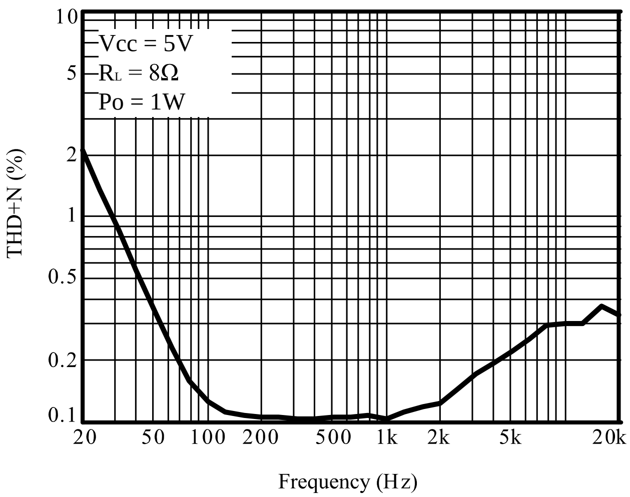


Figure 4 THD+N vs. Frequency

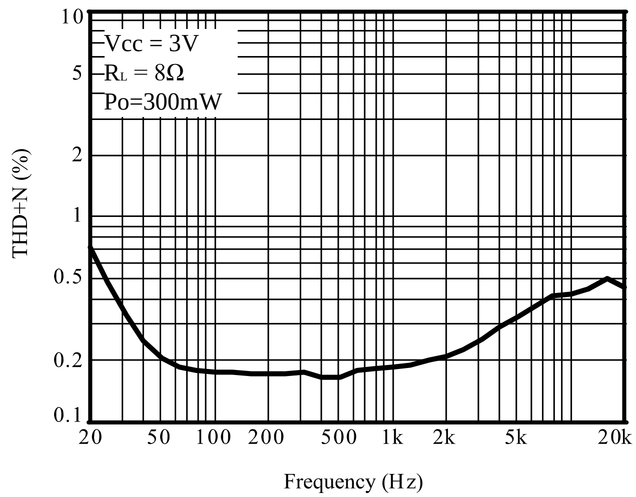


Figure 5 THD+N vs. Frequency

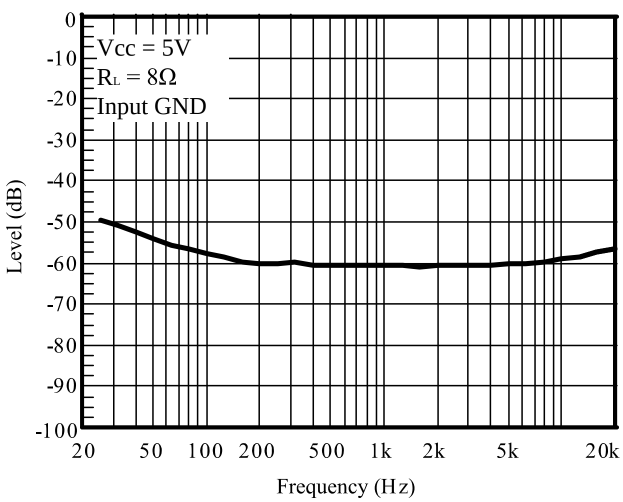


Figure 6 PSRR vs. Frequency

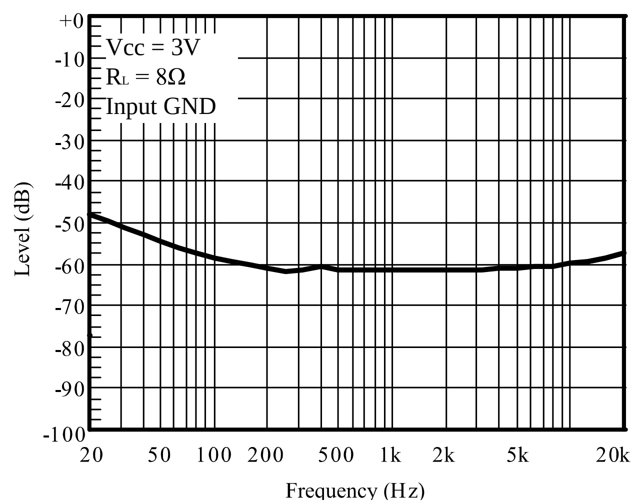


Figure 7 PSRR vs. Frequency

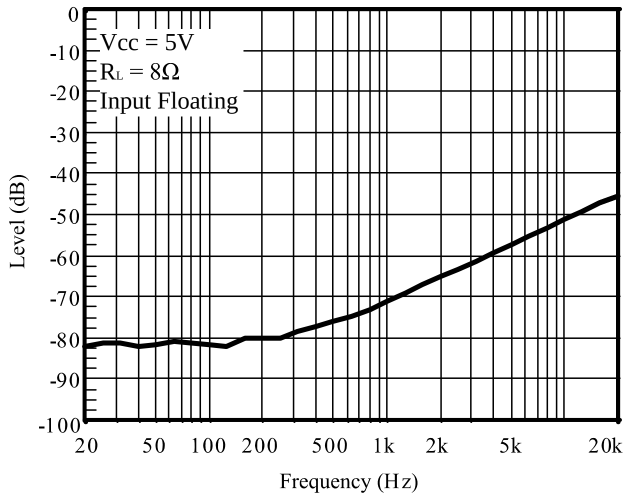


Figure 8 PSRR vs. Frequency

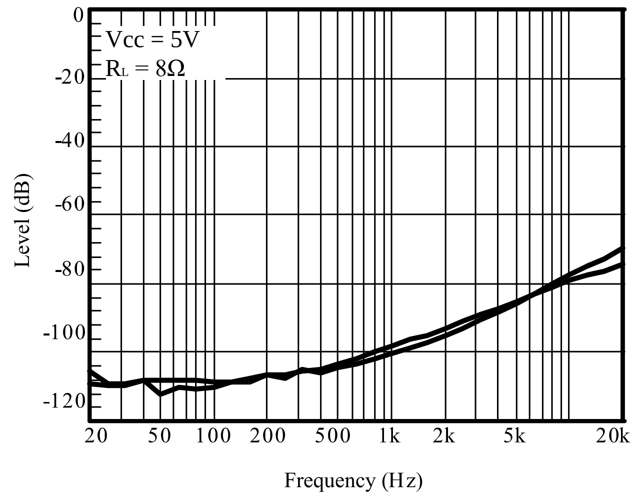


Figure 9 Crosstalk vs. Frequency

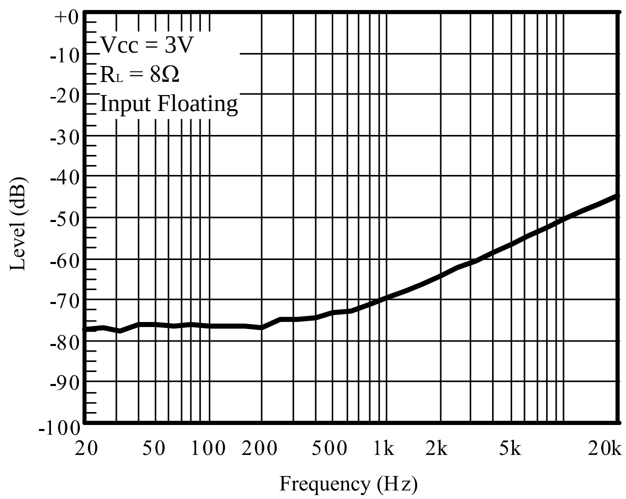


Figure 10 PSRR vs. Frequency

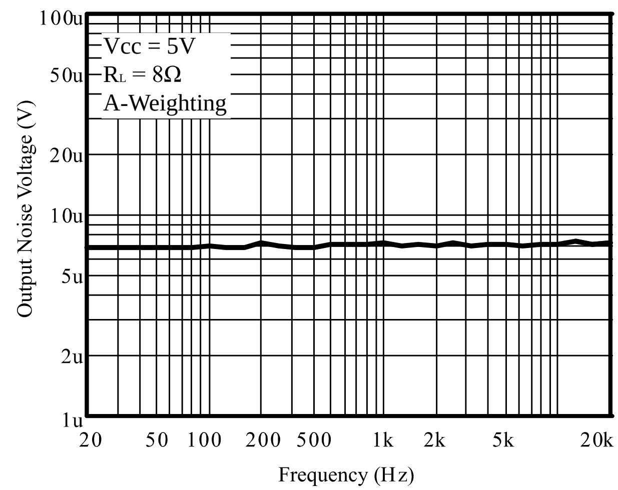


Figure 11 Noise Floor

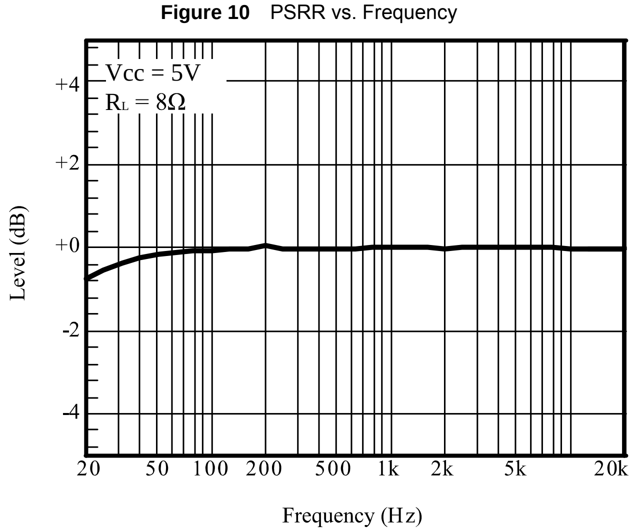


Figure 12 Frequency Response

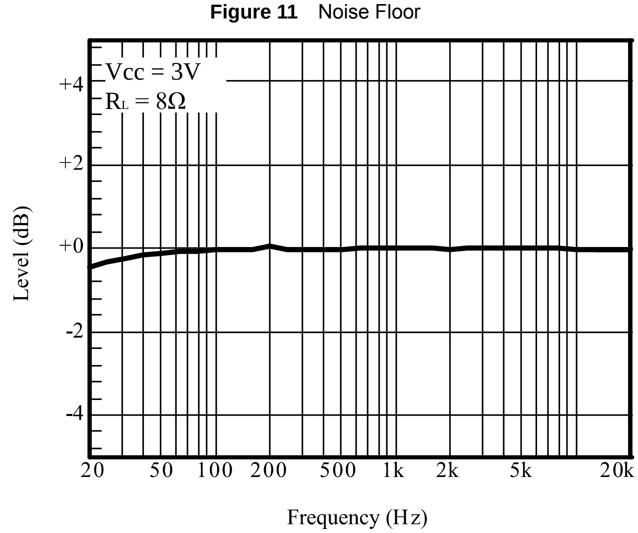


Figure 13 Frequency Response

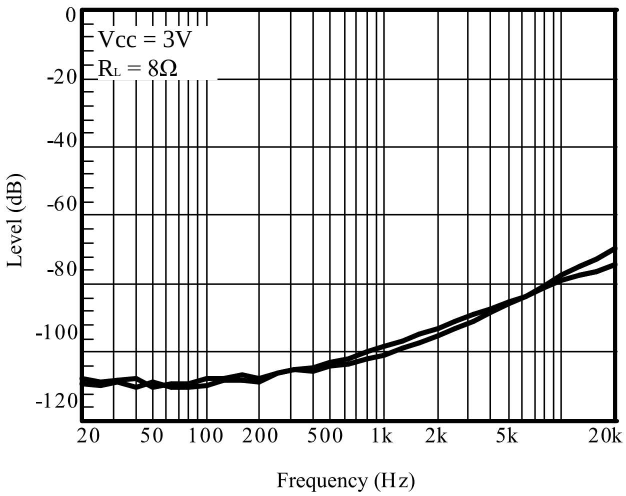


Figure 14 Crosstalk vs. Frequency

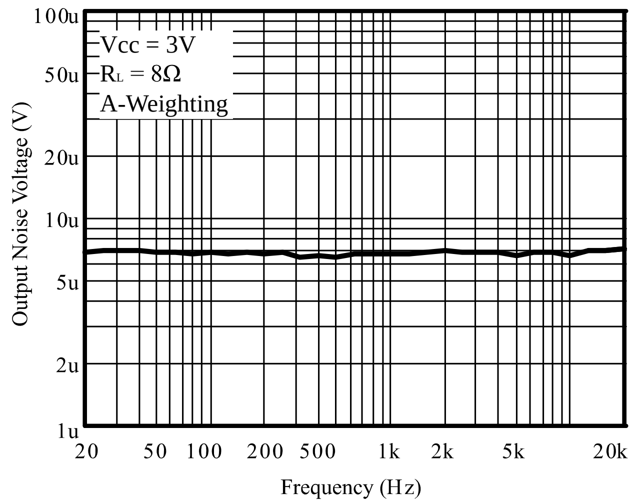


Figure 15 Noise Floor

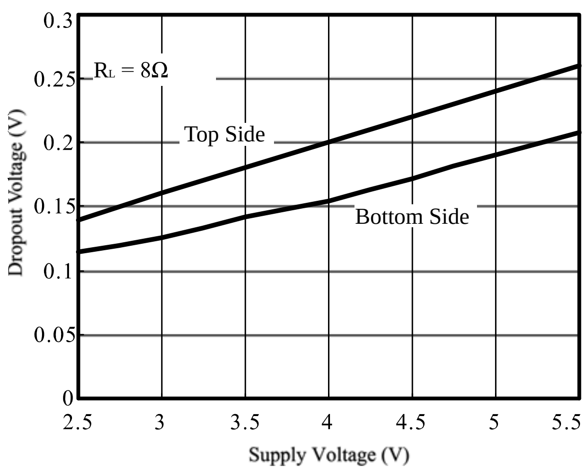


Figure 16 Dropout Voltage vs. Supply Voltage

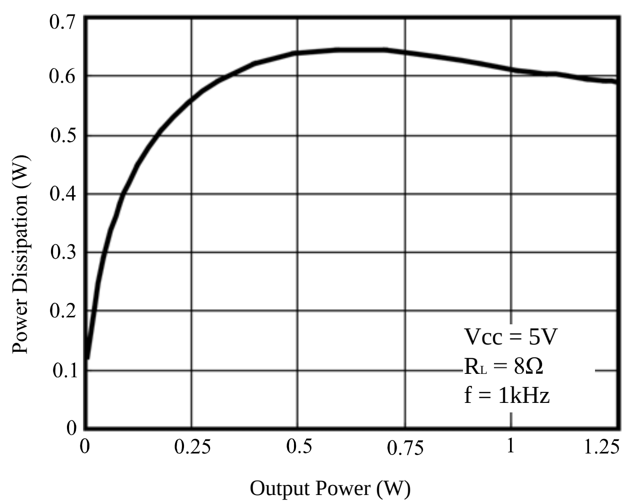


Figure 17 Power Dissipation vs. Output Power

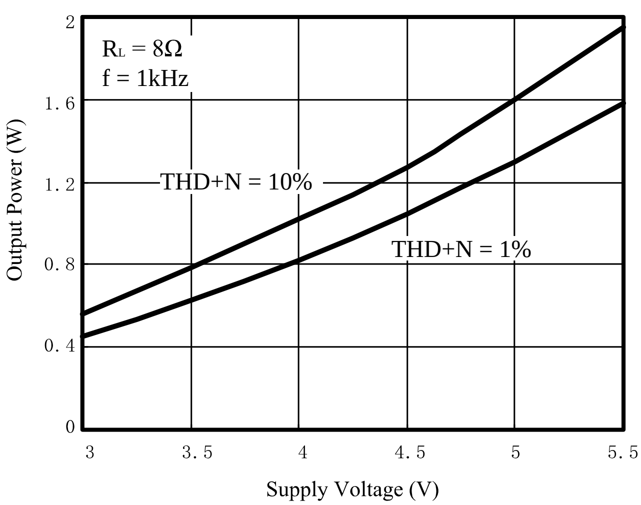


Figure18 Output Power vs. Supply Voltage

APPLICATION INFORMATION

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The IS31AP4066D's QFN (die attach paddle) package provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air.

The QFN package must have it's DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 2, the IS31AP4066D consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. External feedback resistors R_2, R_4 and input resistors R_1 and R_3 set the closed-loop gain of Amp A (-out) and Amp B (-out) whereas two internal 20kΩ resistors set Amp A's (+out) and Amp B's (+out) gain at 1. The IS31AP4066D drives a load, such speaker, connected between the two amplifier outputs, −OUTA and +OUTA.

Figure 2 shows that Amp A's (-out) output serves as Amp A's (+out) input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between −OUTA and +OUTA and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2\times(R_f/R_i) \qquad (1)$$

or

$$A_{VD} = 2\times(R_2/R_1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation (2) states the maximum power dissipation point for a single ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \text{ Single-Ended} \qquad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The IS31AP4066D has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation (3), assuming a 5V power supply and an 8Ω load, the maximum single channel power dissipation is 0.63W or 1.26W for stereo operation.

$$P_{DMAX} = 4\times(V_{DD})^2/(2\pi^2 R_L) \text{ Bridge Mode} \qquad (3)$$

The IS31AP4066D's power dissipation is twice that given by Equation (2) or Equation (3) when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$P_{DMAX}' = (T_{JMAX} - T_A)/\theta_{JA} \qquad (4)$$

The IS31AP4066D's T_{JMAX} = 150°C. In the QFN package soldered to a DAP pad that expands to a copper area of 5in^2 on a PCB, the IS31AP4066D's θ_{JA} is 23°C/W. At any given ambient temperature T_A, use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (4) and substituting P_{DMAX} for P_{DMAX}' results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the IS31AP4066D's maximum junction temperature.

$$T_A = T_{JMAX} - 2\times P_{DMAX}\,\theta_{JA} \qquad (5)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 85°C for the QFN package.

$$T_{JMAX} = P_{DMAX}\,\theta_{JA} + T_A \qquad (6)$$

Equation (6) gives the maximum junction temperature T_{JMAX}. If the result violates the IS31AP4066D's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation (2) is greater than that of Equation (3), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. The θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.)

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitor to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the IS31AP4066D's supply pins and ground. Keep the length of leads and traces that connect capacitors between the IS31AP4066D's power supply pin and ground as short as possible.

MICRO-POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the IS31AP4066D's shutdown function. Activate micro-power shutdown by applying GND to the SHUTDOWN pin. When active, the IS31AP4066D's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The low 0.3µA typical shutdown current is achieved by applying a voltage that is as near as GND as possible to the SHUTDOWN pin.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When use a switch, connect an external 100k resistor between the SHUTDOWN pin and GND. Select normal amplifier operation by closing the switch. Opening the switch sets the SHUTDOWN pin to ground through the 100k resistor, which activates the micropower shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull up resistor.

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the IS31AP4066D's performance requires properly selecting external components. Though the IS31AP4066D operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The IS31AP4066D is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of 1VRMS (2.83VP-P). Please refer to the Audio Power Amplifier Design section for more information on selecting the proper gain.

INPUT CAPACITOR VALUE SELECTION

Amplifying the lowest audio frequencies requires high value input coupling capacitors (C_1 and C_2) in Figure 2. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150 Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

Besides effecting system cost and size, C_1 and C_2 have an effect on the IS31AP4066D's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{DD}/2$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistors, R_2 and R_4. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

A shown in Figure 2, the input resistors (R1 and R3) and the input capacitors (C1 and C2) produce a −3dB high pass filter cutoff frequency that is found using Equation (7).

$$f_{-3dB} = 1/2\pi R_{in}C_{in} = 1/2\pi\ R_1C_1 \qquad (7)$$

As an example when using a speaker with a low frequency limit of 150Hz, C1, using Equation (7) is 0.053µF. The 0.33µF C1 shown in Figure 2 allows the IS31AP4066D to drive high efficiency, full range speaker whose response extends below 30Hz.

BYPASS CAPACITOR VALUE SELECTION

Besides minimizing the input capacitor size, careful consideration should be paid to value of C4, the capacitor connected to the BYPASS pin. Since C4 determines how fast the IS31AP4066D settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the IS31AP4066D's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C4 equal to 1.0μF along with a small value of C1 (in the range of 0.1μF to 0.39μF), produces a click-less and pop-less shutdown function. As discussed above, choosing C1 no larger than necessary for the desired bandwith helps minimize clicks and pops. Connecting a 1μF capacitor, C4, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The IS31AP4066D contains circuitry that minimizes turn-on and shutdown transients or "clicks and pop". For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. When the part is turned on, an internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin.

The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD}. As soon as the voltage on the bypass pin is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of C4 alters the device's turn-on time and the magnitude of "clicks and pops". Increasing the value of C4 reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C4 increases, the turn-on time increases. There is a linear relationship between the size of C4 and the turn-on time. Here are some typical turn-on times for various values of C4 (all tested at V_{DD}=5V):

C_4	T_{ON}
0.01μF	13ms
0.1μF	26ms
0.22μF	44ms
0.47μF	68ms
1.0μF	120 ms

In order eliminate "clicks and pops"; all capacitors must be discharged before turn-on. Rapidly switching V_{DD} on and off may not allow the capacitors to fully discharge, which may cause "clicks and pops".

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

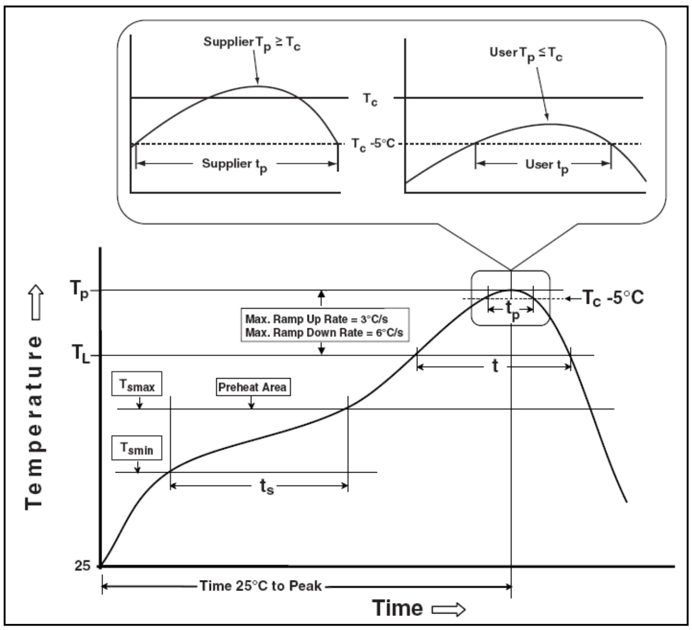
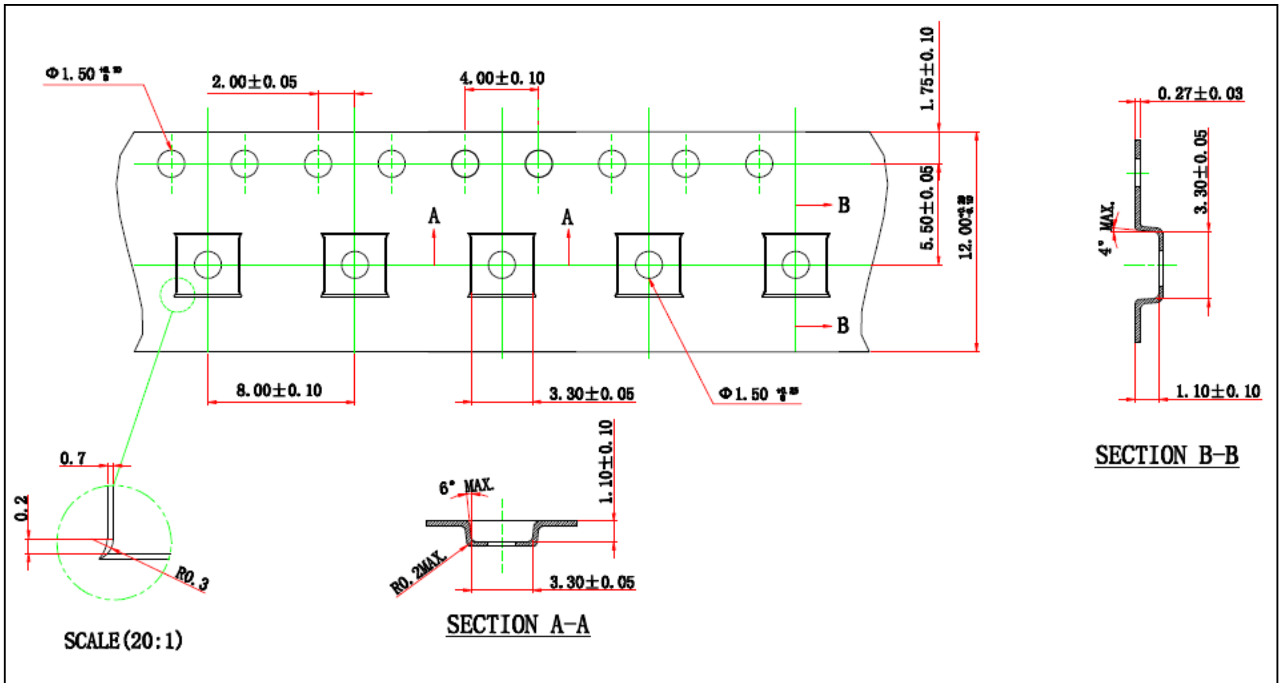


Figure 19 Classification Profile

TAPE AND REEL INFORMATION

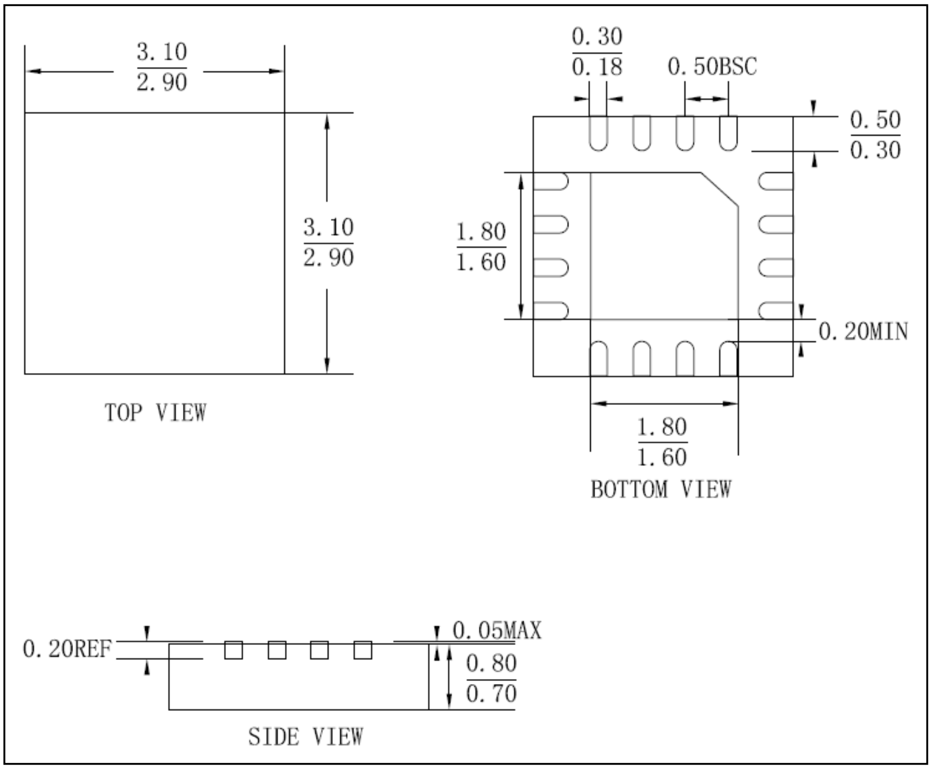


NOTES:

1.CARRIER TAPE COLOR: BLACK
2.COVER TAPE WIDTH: 9.50±0.10
3.COVER TAPE COLOR: TRANSPARENT
4. SURFACE ANTISTATIC COATED 10^{6} ~ 10^{11} OHMS/SQ.
5.10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20MAX.
6.CAMBER NOT TO EXCEED 1 MM IN 100 MM
7.MOLD# WBFBP(3×3)
8.ALL DIMS IN mm.
9.THE DERECTION OF VIEW:

PACKAGE INFORMATION

QFN-16



Note: All dimensions in millimeters unless otherwise stated.